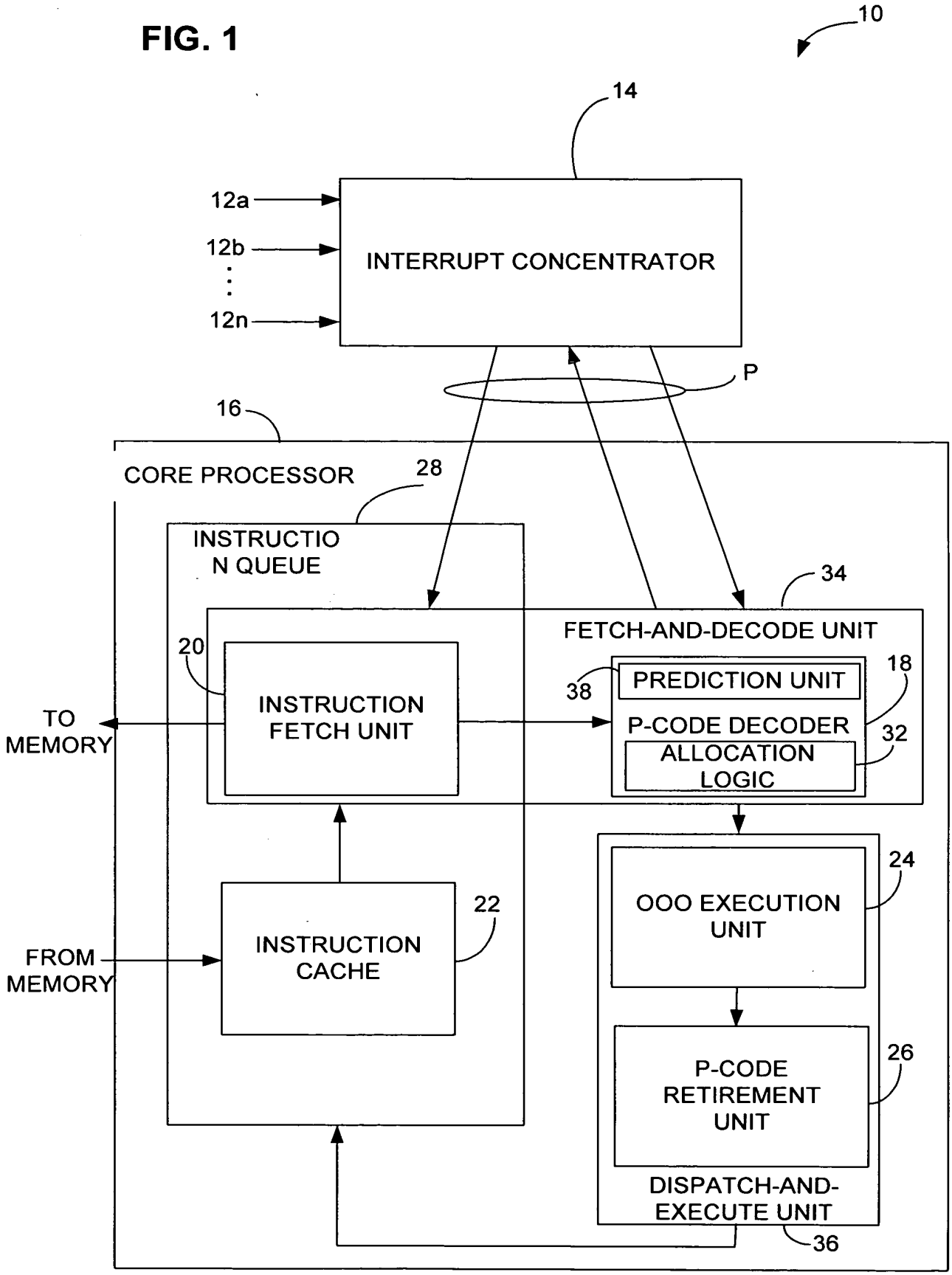
FIG. 1


10
14
12a
12b
12n
INTERRUPT CONCENTRATOR
P
16
CORE PROCESSOR
28
INSTRUCTIO N QUEUE
34
FETCH-AND-DECODE UNIT
20
INSTRUCTION FETCH UNIT
38
PREDICTION UNIT
18
P-CODE DECODER
32
ALLOCATION LOGIC
TO MEMORY
FROM MEMORY
INSTRUCTION CACHE
22
OOO EXECUTION UNIT
24
P-CODE RETIREMENT UNIT
26
DISPATCH-AND-EXECUTE UNIT
36

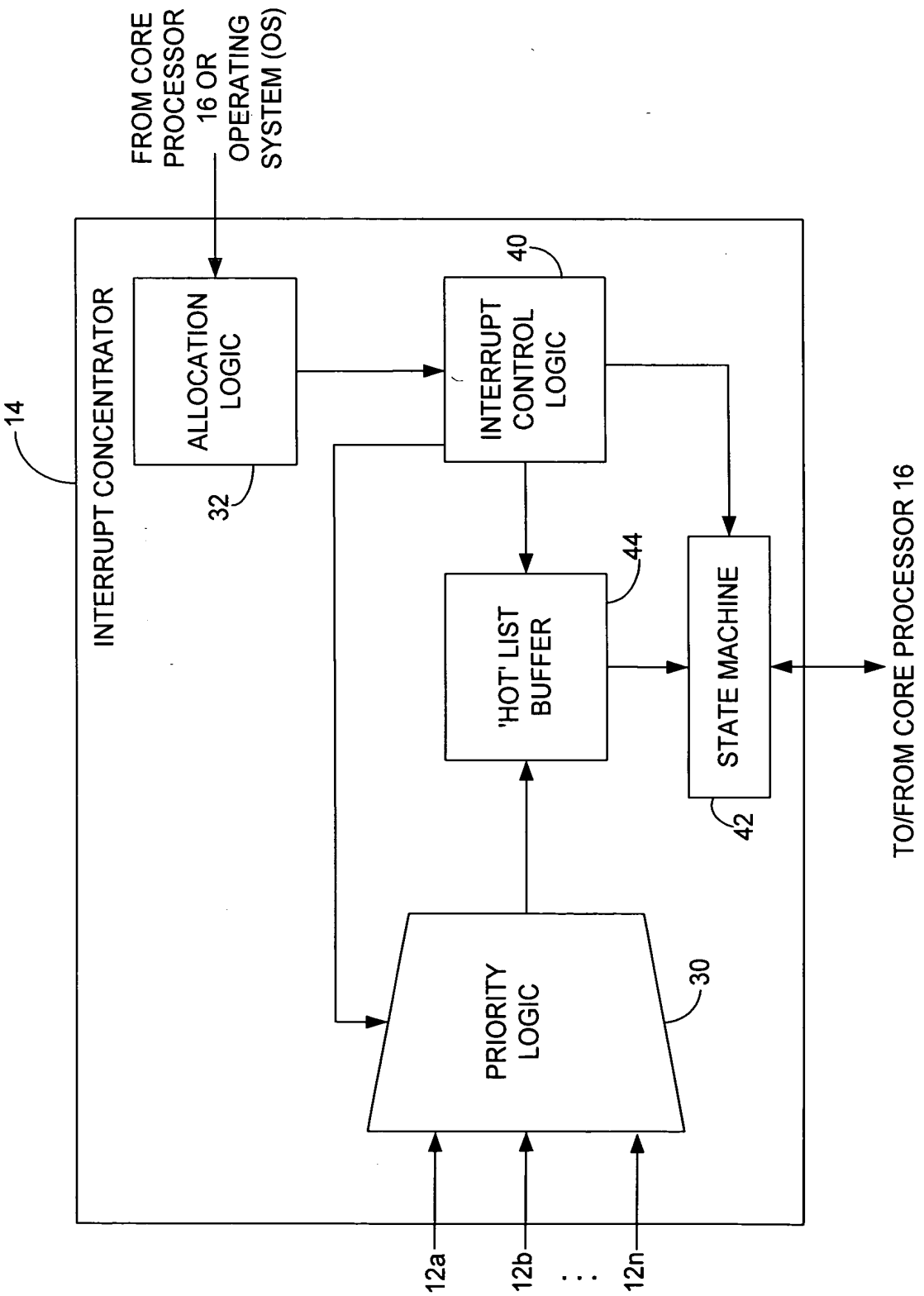

FROM CORE PROCESSOR 16 OR OPERATING SYSTEM (OS)
INTERRUPT CONCENTRATOR
14
ALLOCATION LOGIC
32
INTERRUPT CONTROL LOGIC
40
'HOT' LIST BUFFER
44
STATE MACHINE
42
TO/FROM CORE PROCESSOR 16
PRIORITY LOGIC
30
12a
12b
12n

FIG. 2

FIG. 3A

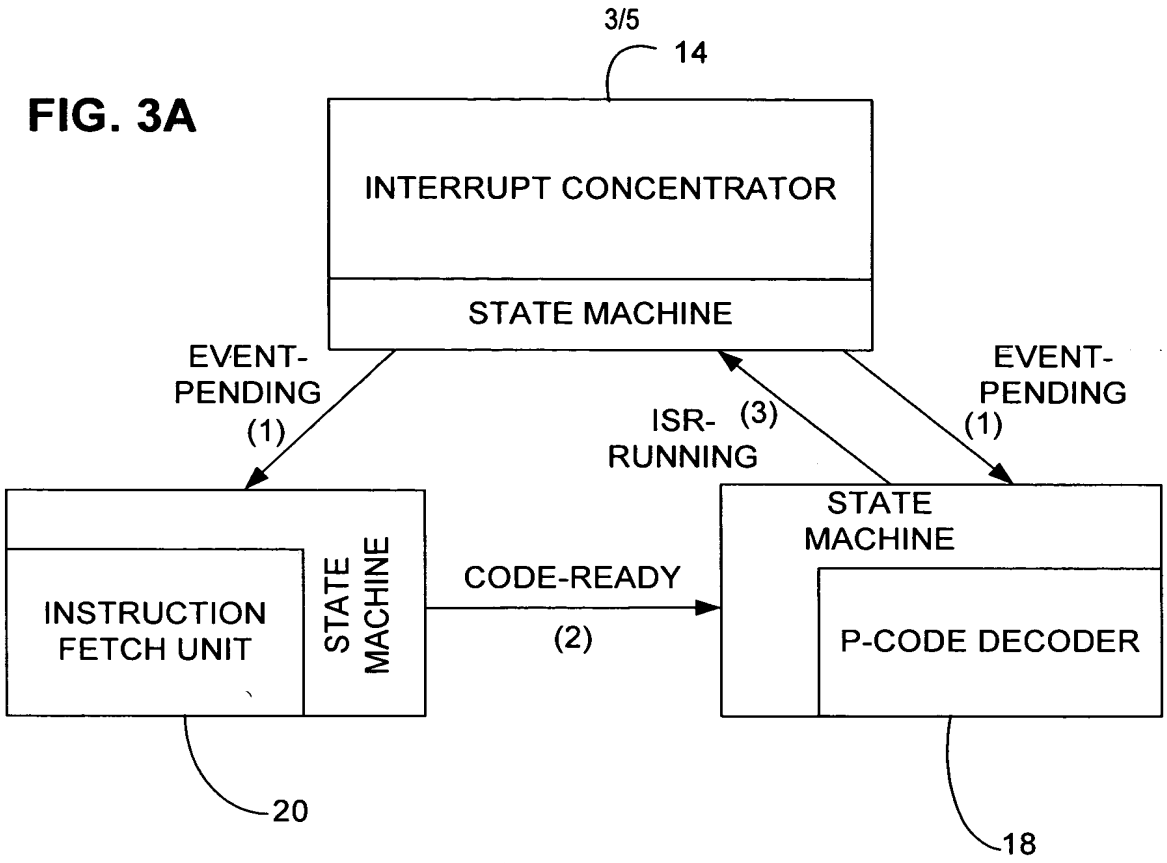
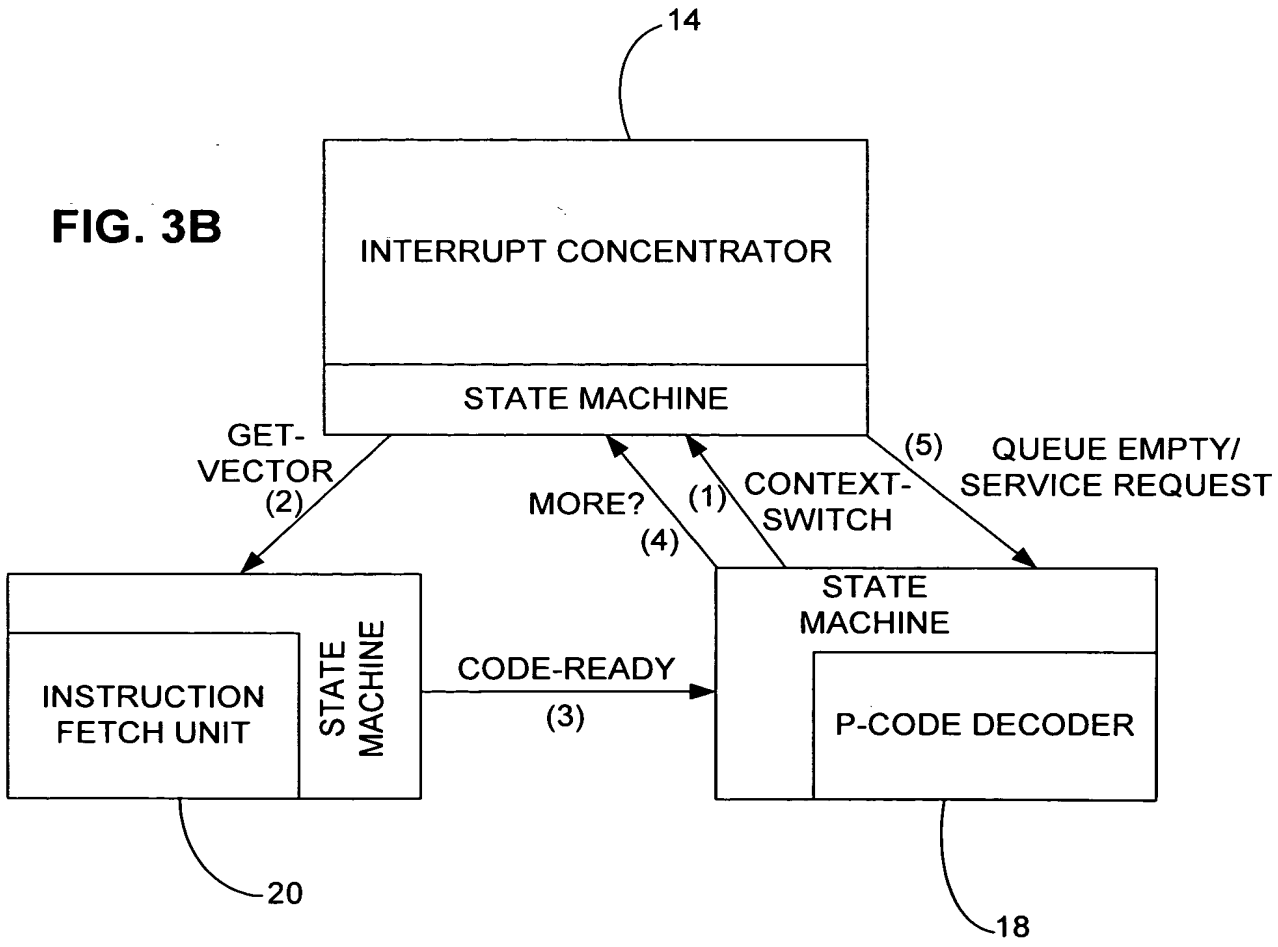

14
INTERRUPT CONCENTRATOR
STATE MACHINE
EVENT-PENDING (1)
ISR-RUNNING (3)
EVENT-PENDING (1)
INSTRUCTION FETCH UNIT
STATE MACHINE
CODE-READY (2)
STATE MACHINE
P-CODE DECODER
20
18

FIG. 3B


14
INTERRUPT CONCENTRATOR
STATE MACHINE
GET-VECTOR (2)
MORE? (4)
(1) CONTEXT-SWITCH
(5) QUEUE EMPTY/ SERVICE REQUEST
INSTRUCTION FETCH UNIT
STATE MACHINE
CODE-READY (3)
STATE MACHINE
P-CODE DECODER
20
18

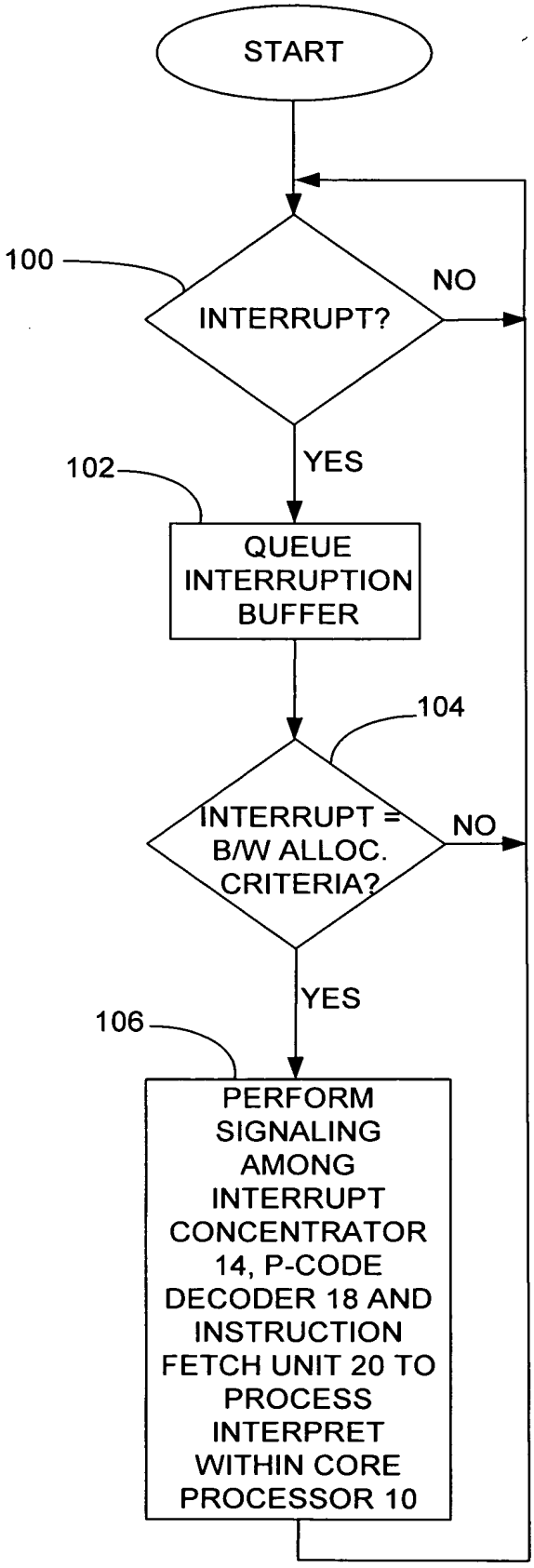

START
100
INTERRUPT?
NO
YES
102
QUEUE INTERRUPTION BUFFER
104
INTERRUPT = B/W ALLOC. CRITERIA?
NO
YES
106
PERFORM SIGNALING AMONG INTERRUPT CONCENTRATOR 14, P-CODE DECODER 18 AND INSTRUCTION FETCH UNIT 20 TO PROCESS INTERPRET WITHIN CORE PROCESSOR 10

FIG. 4

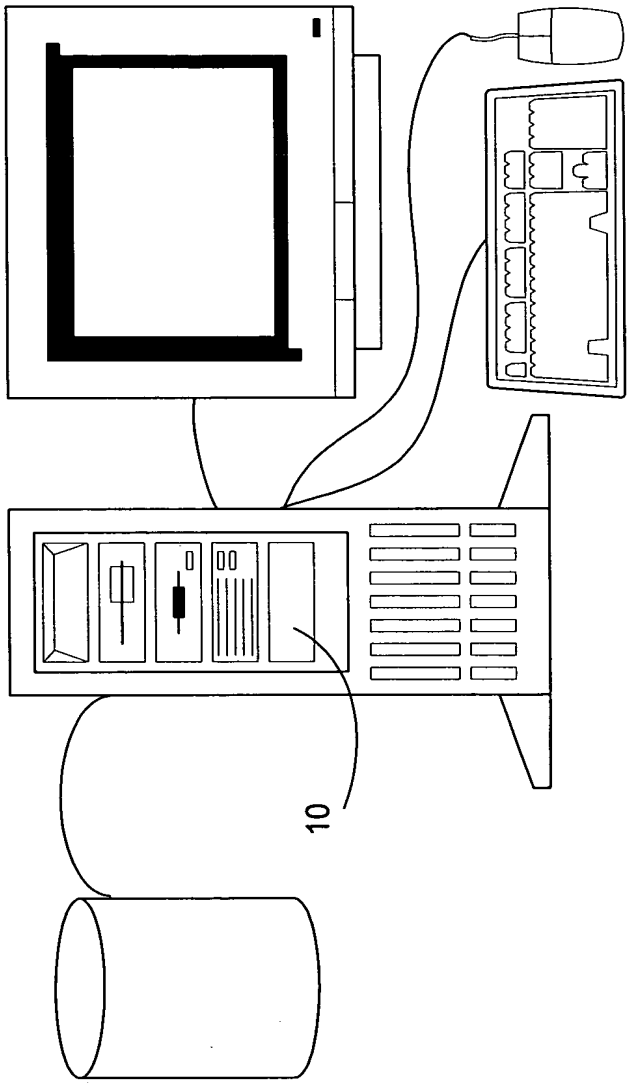


FIG. 5